Notice of Allowability	Application No.	Applicant(s)	
	10/692,416	AIPPERSPACH ET AL.	
	Examiner	Art Unit	
	Khareem E. Almo	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *papaers filed 1/19/2007*.

2. ☒ The allowed claim(s) is/are *1-4,7-17,19 and 22-26*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 12/20/2006
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

QUANTRA
PRIMARY EXAMINER

DETAILED ACTION

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Stephen Walder on 2/20/2007.

Claim 10 line 11 has been changed from "sequentially advancing a clock pulse through delay sub-blocks" to --sequentially advancing the clock pulse through delay sub-blocks--.

Claim 10 line 13 has been changed from "altering a clock pulse that is greater than a predetermined pulse width" to --altering the clock pulse that is greater than a predetermined pulse width--.

Allowable Subject Matter

2. Claims 1-4, 7-9, 10-17, 19, 22-26 are allowed.

With respect to claims 1-4, 7-9 and 24-26, the prior art of record fails to suggest or disclose a pulse width limiting circuit wherein the high low clock pulse shuttle shunts the unconditioned clock signal to the block delay module if a clock pulse width of the unconditioned clock signal is outside a pulse width limit and wherein the unconditioned

clock signal is passed as a corrected clock output signal if the clock pulse width of the unconditioned clock signal is equal to or less than the pulse width limit by bypassing the high low clock pulse shuttle circuit.

With respect to claims 10-17, 19 the prior art of record fails to disclose or suggest the method as recited comprising the step wherein injecting the clock pulse through a block delay module in response to the clock shuttle node identifying a clock pulse width of the clock pulse as being outside a predetermined pulse width limit; in combination with the step of substantially passing through the clock pulse by bypassing the clock shuttle node in response to the clock pulse width of the clock pulse being less than or equal to the predetermined pulse width limit.

With respect to claim 22, the prior art of record fails to suggest or disclose a method of providing a pulse width limiting circuit comprising the step of providing a high low clock pulse shuttle circuit, coupled to the clock signal correction block, configured to accept the conditioned clock signal wherein the high low clock pulse shuttle comprises a first FET coupled to the correction block wherein the high low clock pulse shuttle circuit shunts the unconditioned clock signal to the block delay module if a clock pulse width of the unconditioned clock signal is outside a pulse width limit and wherein the unconditioned clock signal is passed as at he corrected clock output signal if the clock pulse width of the unconditioned clock signal is equal to or less than the pulse width limit by bypassing the high low clock pulse shuttle circuit.

With respect to claim 23, the prior art of record fails to disclose or suggest a high low clock pulse shuttle circuit coupled to the correction block wherein the high low clock

pulse shuttle circuit shunts the clock pulse to the block delay module if a clock pulse width of the clock pulse is outside a pulse width limit and wherein the high low clock pulse shuttle circuit is bypassed if the clock pulse width of the clock pulse is equal to or less than the pulse width limit.

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khareem E. Almo whose telephone number is (571) 272-5524. The examiner can normally be reached on Mon-Fri (8:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

KEA
2/20/2007

Quan Tra
Primary Examiner